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10/629,378	07/28/2003	Graham Kirsch	501278.02	6536

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,378	KIRSCH, GRAHAM	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12,and 19-30* is/are allowed.

6)☒ Claim(s) *13-18 and 31-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-15,17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kashiyama et al. (patent No. 5,247,695).

3. Kashiyama taught (as per claim 13) the invention as claimed including a data processing ("DP") system comprising:

a) A vector processing and reordering system (e.g., see figs.1, 3)(e.g., see col. 3, line 27-col. 4, line19);

b) A vector register (4) receiving data that may be other than a contiguous order (e.g., see fig. 1,3,4)(e.g., see col. 4, lines 1-62);

c) A vector memory (2) coupled to the vector register to store data transferred from the vector register and to pass data stored in the vector memory to the vector register; and (e.g., see figs. 1,3,4, and col. 4, lines 1-62); and

d) A vector processor (1,3,7,9,10,12), coupled to the vector memory to receive data from the vector memory, the vector processor being operable to re-order the data received from the vector memory into a vector of contiguous data, process the data to provide results data and pass the results data to the vector memory (e.g., see fig. 1 and col. 4, lines 37-62).

4. As per claim 14, Kashiyama taught a addressing engine (1) coupled to the vector memory, the addressing engine being operable to control the locations in which data are stored in the vector memory (e.g,. see fig. 1 and col. 3, lines 30-56).

5. As per claim 15, Kashiyama taught the addressing engine is operable to selectively control the address sequence applied to the vector memory as data coupled to or from the vector memory to reorder the data coupled to or from the vector memory (e.g., see figs. 1,2,3,4 and col. 4, lines 37-42 and col. 5, lines 5-24).

6. As per claim 17, Kashiyama taught the vector memory (1) is a random access memory (e.g., see figs. 3-68) .

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashiyama as applied to claims 13 above, and further in view of Iobst (patent No. 5,396,641).

8. As per claim 18, Iobst taught the vector processor comprises an arithmetic logic unit (38) (e.g., see col., 4, lines 29-49) and a register (R register) coupled to receive and store data resulting from an arithmetic or logical operation performed by the arithmetic and logic unit (e.g., see figs. 1, 2 and col. 3, line 55-col. 4, line 14).

9. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Kashiyama and Iobst. Both references were directed toward selectively processing vector data in a DP system. One of ordinary skill would have been motivated to incorporate the Iobst teachings of the process comprising an arithmetic logic unit at least to facilitate the selective processing of more varied types of functions such as logic functions along with arithmetic functions.

10. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashiyama as applied to claims 13 above, and further in view of van Hook (patent No. 6,266,758).

11. As per claim 16, van Hook taught the vector memory comprises a dual port memory, one of the ports being coupled to the vector register and the other of the ports of the vector memory being coupled to the vector processor [the vector main memory with the vector load store unit comprises dual ports for transferring data between the Vector processor (316) and the vector register file (304) (e.g., see fig. 3 and col. 5, line 15-col. 6, line 21)].

12. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Kashiyama and van Hook. Both references were directed toward selectively processing vector data in a DP system. One of ordinary skill would have been motivated to incorporate the van Hook teachings of plural inputs and output to the vector memory unit at least to allow the system to transfer data to or from the registers and memory while the memory is transferring data to or from the processor. This would

reduce the times when memory or vector registers were accessed and the most current data was not available.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 31-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Iobst (patent No. 5,396,641).

15. Iobst taught (as per claim 31) the invention as claimed including a data processing ("DP") system comprising:

a) Storing data in an array of memory cells (6) in the integrated circuit (e.g., see figs.1, 4 and col. 2, lines 11-29);

b) In response to a memory command, reading data from the memory cells in the integrated circuit (e.g., see col. 5, lines 21-50);

c) Re-ordering the data read from the memory cells in the integrated circuit, the reordering occurring in the integrated circuit (e.g., see fig. 3 and col. 7,lines 41-68)[the selector reorders data received from memory for input to a processor];

d) Processing the re-ordered data in the integrated circuit (e.g., see figs. 1,4 and col. 7, lines 41-68).

16. As per claims 32,33 Iobst taught writing processing data to the memory in the integrated circuit and the memory cells comprises standard random access memory

cells (e.g., see col. 2, lines 11-29 and col. 1, lines 30-41) [further dynamic random access memory is within the scope of standard random access memory array (e.g., see co.. 3, lines 25-41) taught by Iobst that comprises dynamic random access cells].

17. As per claim 34,35,36,37 Iobst taught the reordered data in the integrated circuit comprises parallel processing the reordered data comprising single instruction multiple data processing the re-ordered data (e.g., see fig. 4 and col. 4, lines 23-34) by separately processing groups of columns of memory cells (e.g, see fig. 4 and col. 4, lines 15-22 and col. 7, lines 18-68) selecting predetermined portions of the data from memory cells (e.g., see fig. 4 and col. 7, lines 26-57).

18. As per claim 38, Iobst taught the act of storing data in an array of memory cells in the integrated circuit comprises coupling the data to the array of memory cells from an external data port (e.g., see col. 5, lines 51-68).

19. As per claim 39, Iobst taught in an integrated circuit active memory device (e.g., see col. 1, line 63-col. 2, line 10) having an array of memory cells and an array of processing elements (e.g., see fig. 4) each of which is coupled to a respective group of memory cells (e.g., see col. 7,lines 18-57), a method of processing data in the active memory device, comprising reordering data read from the memory cells in a predetermined manner before processing the data in the integrated circuit active memory device to obtain results data (e.g., see fig. 3 and col. 7,lines 41-68).

Claim Rejections - 35 USC § 103

20. Claims 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over of lobst (patent No. 5,396,641) as applied to claims 39 above, and further in view Kashiyama (patent No. 5,247,695).

21. As per claim 40 Kashiyama taught reordering the results data and storing the results data in the memory cells (e.g., see fig.1) [the results data is shifted before stored in the memory (e.g., see col. 4, lines 44-62).

22. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of lobst and Kashiyama. Both references were directed toward selectively processing vector data in a DP system. One of ordinary skill would have been motivated to incorporate the Kashiyama teachings of the process selectively shifting data before and after processing at least to provide a more flexible processing of data from particular portions of data that is processed and stored in memory.

Allowable Subject Matter

Claims 1-12 and 19-30 allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Morton (patent No. 5,822,606) disclosed a DSP having plurality of like processors controlled in parallel (e.g., see abstract).

Ansari (patent No. 6,813,701) disclosed a system for transferring vector data between memory and register file (e.g., see abstract).

Dowling (patent No. 6,226,738) disclosed a split embedded dram processor (e.g., see abstract).

Resnick (patent No. 6,295,597) disclosed a system for improved vector processing to support extended-length integer arithmetic (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ERIC COLEMAN
PRIMARY EXAMINER